SCP1853
SCP1853L

Preliminary

μMOS 1800 FAMILY

Solid State Scientific, Inc.

I/O Expander

Silicon Gate CMOS

Features

- Directly Compatible with SCP1802 Microprocessor
- Expands SCP1802's Peripheral Selection Control
- 3-to-8 Decoder
- Standard CMOS Advantages:
  - High noise immunity
  - Very low power
  - Wide temperature range
- Static Circuitry

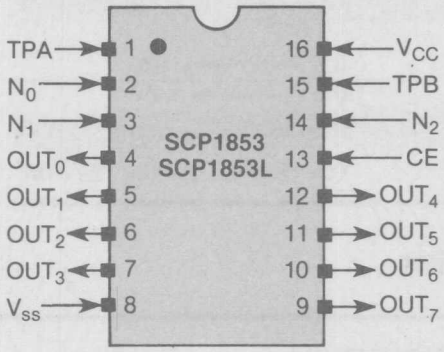
Description

The SCP1853 I/O Expander is designed to increase the peripheral addressing capability of the SCP1802 microprocessor. As inputs, it takes the 1802's three N-lines (N_{0-2}) and two timing pulses (TPA, TPB). These N-lines are used to select the desired I/O Port (SCP1852) or other peripheral; the SCP1853 I/O Expander decodes the 3 N-lines to provide a one-of-eight signal (OUT_{0-7}).

A Chip Enable (CE) input allows for multilevel I/O configurations. Also, the SCP1802's TPA and TPB are used to capture valid data (TPA) and to enable the outputs (TPB).

The SCP1853 comes in standard 16-pin packages. The SCP1853 and SCP1853L are functionally identical; they differ in their operating voltage range.

Pin Configuration



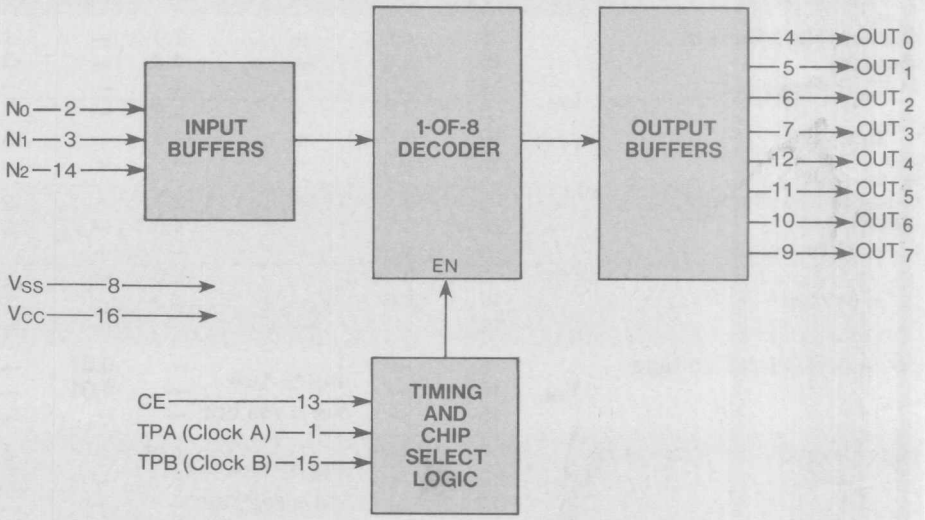
Pin Names

N_{0-2}	SCP1802 N-Lines
OUT_{0-7}	Outputs
TPA, TPB	Timing Pulses
CE	Chip Enable

Suffixes

L	4-6V operating range
no L	4-12V operating range
D	ceramic
C	cerdip
E	epoxy
H	chip

Block Diagram



DEVICE SPECIFICATIONS

Recommended Operating Conditions

PARAMETER		SCP1853	SCP1853L	UNITS
DC Supply Voltage	V_{CC}	4-12	4-6	V
Operating Temperature:				
D, C, H devices	T_A	-55 → +125		°C
E device		-40 → +85		

Absolute Maximum Limits

PARAMETER		VALUE
Storage Temperature	T_S	-65° → +150°C
DC Supply Voltage:		
SCP1853	V_{CC}	-0.5 → +15V
SCP1853L		-0.5 → +7V
Power Dissipation (per Package)	P_T	500mW
Input Voltage	V_{IN}	$V_{SS} \leq V_{IN} \leq V_{CC} \leq V_{DD}$[1]

CE	TPA	TPB	EN[4]
1	0	0	*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

* EN remanins in previous state.

INPUTS				OUTPUTS							
N_2	N_1	N_0	EN	0_0	0_1	0_2	0_3	0_4	0_5	0_6	0_7
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

Fig. 1 SCP1853 Truth Tables

Static Electrical Characteristics

V_{SS} = 0 V

PARAMETER		CONDITIONS[2]			T_{LO}[3]		+ 25°C			T_{HI}[3]		UNITS
		V_{CC}	V_O	Other	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device Current:		5	—	—	—	0.1	—	0.001	0.05	—	1.5	
		10	—	—	—	0.5	—	0.005	0.10	—	3.0	mA
SCP1853	I_L	15	—	—	—	1.0	—	0.010	0.50	—	15.0	
SCP1853L		5	—	—	—	0.5	—	0.005	0.10	—	3.0	
Outputs High Current (Source):		5	4.6	—	-2.0	—	-1.6	-3.0	—	-1.1	—	
		10	9.5	—	-4.4	—	-3.6	-6.5	—	-2.5	—	
C, D, H devices	I_{OH}	15	13.5	—	—	—	—	-14.0	—	—	—	mA
		5	4.6	—	-1.9	—	-1.6	-3.0	—	-1.2	—	
E device		10	9.5	—	-4.3	—	-3.6	-6.5	—	-2.8	—	
		15	13.5	—	—	—	—	-14.0	—	—	—	
Outputs Low Current (Sink):		5	0.4	—	2.7	—	2.2	4.5	—	1.6	—	
		10	0.5	—	4.5	—	3.6	7.5	—	2.5	—	
C, D, H devices	I_{OL}	15	1.5	—	—	—	—	16.5	—	—	—	mA
		5	0.4	—	2.6	—	2.2	4.5	—	1.8	—	
E device		10	0.5	—	4.3	—	3.6	7.5	—	2.8	—	
		15	1.5	—	—	—	—	16.5	—	—	—	
Low-Level Output Voltage		5	—		—	0.01	—	0.0	0.01	—	0.05	
	V_{OL}	10	—	$\lvert I_O \rvert \leq 1\mu A$	—	0.01	—	0.0	0.01	—	0.05	Vdc
		15	—	$V_{IN} = V_{SS}, V_{CC}$	—	—	—	0.0	—	—	—	
High-Level Output Voltage		5	—		4.99	—	4.99	5.0	—	4.95	—	
	V_{OH}	10	—	$\lvert I_O \rvert \leq 1\mu A$	9.99	—	9.99	10.0	—	9.95	—	Vdc
		15	—	$V_{IN} = V_{SS}, V_{CC}$	—	—	—	15.0	—	—	—	
Input Low Voltage		5	.5,4.5		1.5	—	1.5	2.25	—	1.5	—	
	V_{IL}	10	1,9	$\lvert I_O \rvert \leq$	3.0	—	3.0	4.50	—	3.0	—	Vdc
		15	1.5,13.5	$1\mu A$	—	—	—	6.75	—	—	—	
Input High Voltage		5	.5,4.5		—	3.5	—	2.75	3.5	—	3.5	
	V_{IH}	10	1,9	$\lvert I_O \rvert \leq$	—	7.0	—	5.50	7.0	—	7.0	Vdc
		15	1.5,13.5	$1\mu A$	—	—	—	8.25	—	—	—	
3-State Output		5	—	$V_{IN} = 0,5$	—							
Leakage Current	I_{ZL}	10	—	$V_{IN} = 0,15$	—	±2.0	—	$\pm 10^{-5}$	±2.0	—	±20.0	μA

Dynamic Electrical Characteristics

$t_R = t_F = 10nS$; $C_L = 100pF$; $T_A = 25°C$

PARAMETER		V_{CC}[2]	MIN.	TYP.	MAX.	UNITS
Total Power Dissipation	P_D	5	—	1.0	—	mW
		10	—	6.0	—	
		15	—	—	—	
Propagation Delay Times: CE to Outputs	t_{EOH}, t_{EOL}	5	—	200	—	nS
		10	—	100	—	
		15	—	—	—	
N to Outputs	t_{NOH}, t_{NOL}	5	—	250	—	nS
		10	—	120	—	
		15	—	—	—	
Clock A to Outputs	t_{AO}	5	—	225	—	nS
		10	—	110	—	
		15	—	—	—	
Clock B to Outputs	t_{BO}	5	—	200	—	nS
		10	—	100	—	
		15	—	—	—	

SCP1802-SCP1853 Interface

Figure 2 shows the interconnection of an SCP1802 and an SCP1853 for one-level I/O selection. As described above, the N lines generate an output (from the SCP1853) which in turn selects the desired peripheral. This configuration permits up to 14 peripherals.

Two-level I/O allows addressing of hundreds of peripheral devices. Fig.4 shows a configuration capable of addressing up to 784 peripherals, 392 inputs and 392 outputs. The SCP1853 Ⓐ and SCP1852 Ⓑ together select one blank of I/O ports; each bank consists of an SCP1853 and up to 14 SCP1852s, as shown.

Two I/O instructions are required: an output to select a bank, followed by the user's input or output instruction. During the first output instruction, the N lines (decoded by Ⓐ) will select one of seven SCP1852s Ⓑ; the byte that is output then selects one of eight banks. The next I/O instruction is therefore directed to the bank of peripherals containing the desired port.

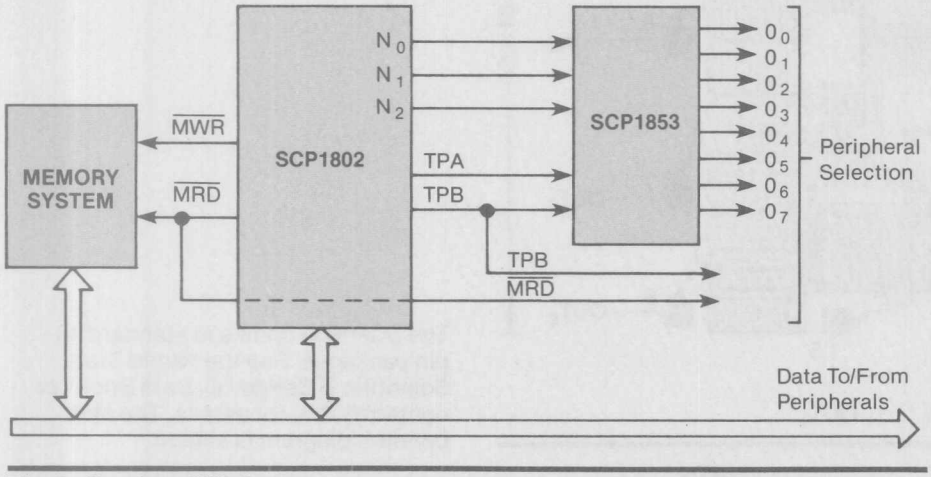


Fig. 2 One Level I/O System

SCP1853 Device Operation

The SCP1853 is intended to interface between the SCP1802 microprocessor and peripheral input/output devices. The SCP1802's N lines (N_{0-2}) are used to select the desired peripheral during execution of I/O instructions (61-67, 69-6F). Since there are 3 N lines, only 6 devices (3 input and 3 output) can be directly selected by the 1802; this limits the use of the 14 I/O instructions (7 input and 7 output). The SCP1853 decodes these N lines into a 1-of-8 signal allowing all 14 instructions to be used and therefore allow up to 14 peripherals (7 input and 7 output).

When the SCP1853 I/O Expander is enabled (CE = 1), the selected output will be high from the falling edge of TPA to the falling edge of TPB; the outputs are 0 at all other times. Chip Enable allows for expanded systems, as shown in Figure 4.

The SCP1853 can also be used as a general 1-of-8 decoder by connecting TPA to V_{SS} and TPB to V_{CC}.

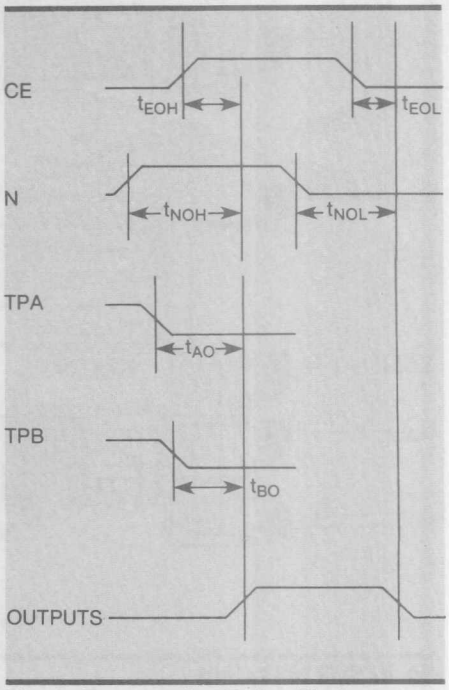


Fig. 3 Propagation Delay Timing Diagrams

1. See SCP1802 data sheet for V_{DD} specifications.
2. For SCP1853L, use 5V specs only.

3. Device	T_{LO}	T_{HI}
C, D, H	-55°C	+125°C
E	-40°C	+85°C

4. Enable (EN) is an internal signal (see Block Diagram). Outputs are enabled when EN = 1.

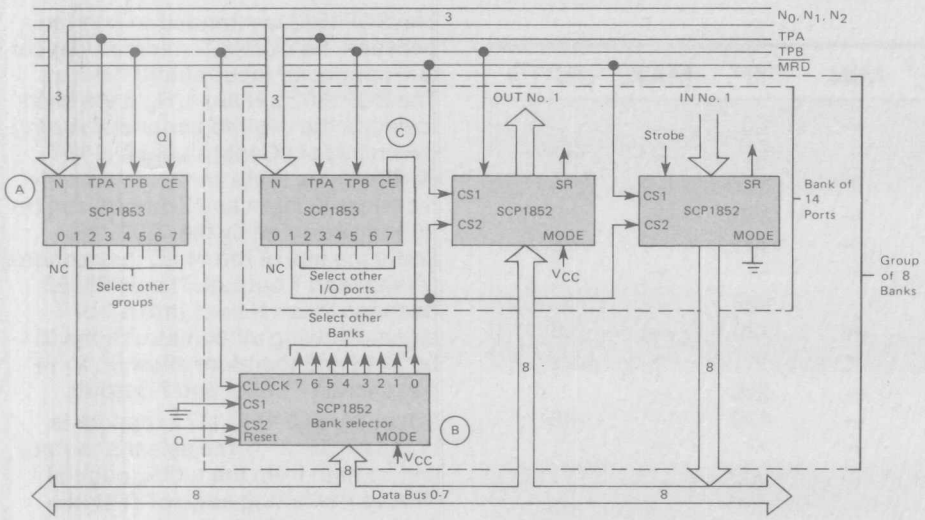


Fig. 4 - Two Level I/O Selection

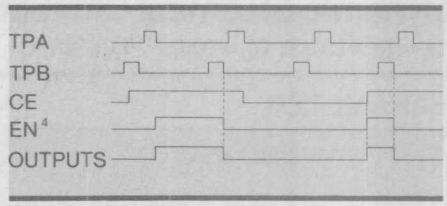


Fig. 5 SCP1853 Timing Diagram

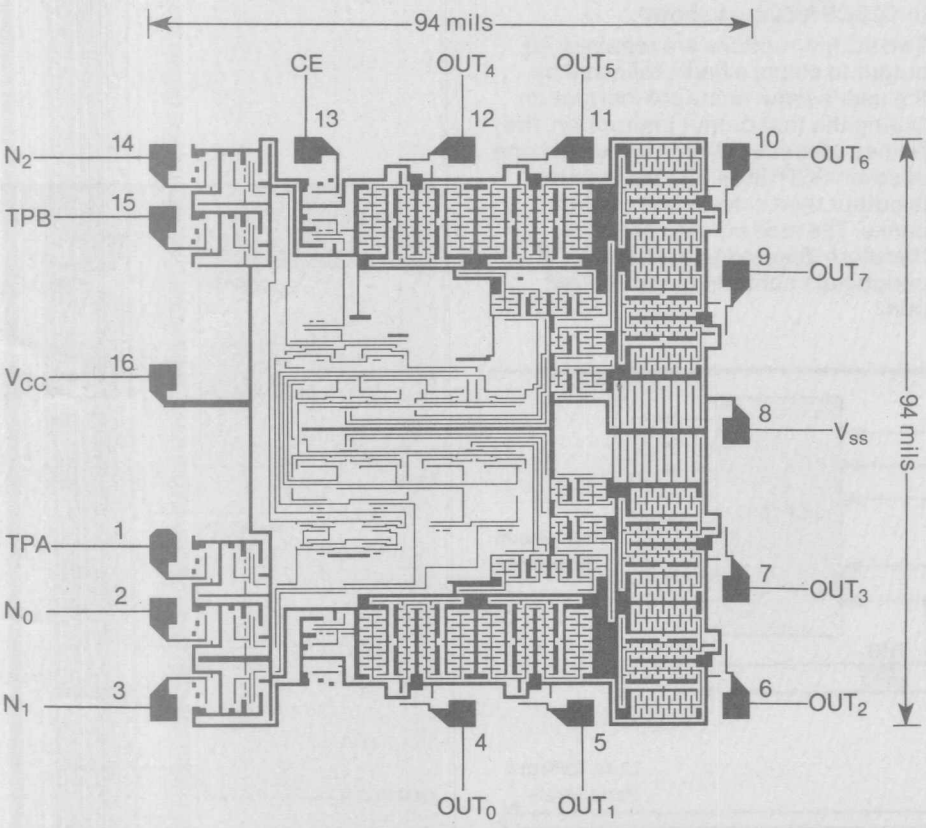


Fig. 6 SCP1853 Chip

The SCP1853 comes in standard 16-pin packages. See the "Solid State Scientific B-Series I.C. Data Book" or contact S.S.S. for details. The chip bonding diagram is shown.

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